REMARKS

Claims 9-12 and 24 are presently pending in the application. Claim 24 has been added. Reconsideration and allowance of all claims are respectfully requested in view of the following remarks.

The Examiner has rejected Claims 9-12 under 35 U.S.C. §103 as being unpatentable over Eda et al. For the following reasons, the prior art rejection is respectfully traversed.

The present invention relates to nitride III-V compound semiconductor device for high-frequency operation, which uses a thinned single-crystal substrate, such as a sapphire or SiC substrate, and/or the use of a via hole in such a substrate to achieve reduce operation voltage etc.

Eda et al. disclose a semiconductor substrate having an FET formed thereon, and with electrical connection of the lower electrode of the resonator and the wiring formed on the semiconductor substrate being made through a via-hole method.

The Applicant respectfully submits that Eda et al. do not teach or suggest a single-crystal substrate made of a material different from nitride III-V compound semiconductors, and a device formed on one major surface of said single-crystal substrate by using III-V compound semiconductors, wherein electrical connection to said device is made through a via hole formed in said single-crystal substrate, as recited in amended Claim 9.

Rather, contrary to the Examiner's assertion, Eda et al. disclose in most embodiments, only a silicon substrate 1 and do not list the type or materials of the semiconductor device or of the FET. Rather, it can only be assumed that the material used is usable with a silicon substrate. In other embodiments, when a GaAs II-V group compound semiconductor is disclosed, the substrate is also disclosed as GaAs or InP in Eda et al.

However, in order to establish a *prima facie* case of obviousness, the Examiner must show some suggestion or motivation in the Eda et al. reference, or in the knowledge generally available to one of

ordinary skill in the art, to modify the reference to result in the claimed features of the present invention. Second, there must be a reasonable expectation of success, and finally, Eda et al. must teach or suggest all the claim limitations.

Eda et al. fails in all respects as there is no teaching or suggestion in the reference that the III-V group compound semiconductors are used with a substrate that is a single crystal and different in material from that of the III-V group compound semiconductors, nor does Eda et al. disclose that there would be a reasonable expectation of success if that were the case.

Further, as with Eda et al. and in the state of the art, when nitride III-V compound semiconductors are used, the substrate material is usually in that group, such as GaN, or GaAs, etc., since as stated in the Background of the Invention section of the present specification, single crystal substrates present problems in manufacturing when used with a nitride III-V compound semiconductor device.

However, in the present invention, the use of a single crystal material for the substrate which is different from the nitride III-V compound semiconductor is nonobvious since the single crystal material must be manufactured by a special process in order to be appropriately thinned for use with a nitride III-V compound semiconductor. Further, the resulting enhanced properties of the semiconductor device when the claimed materials are used, possess unexpectedly advantageous and superior properties, such as reduced operation voltage etc.

Accordingly, Claim 9 is not obvious over Eda et al., and the rejection of Claim 9 under 35 U.S.C. §103 should be withdrawn.

With respect to Claim 10, the Applicant respectfully submit that Eda et al. do not teach or suggest a semiconductor device as in Claim 9, wherein the substrate is one of a sapphire substrate, spinel substrate, perovskite yttrium aluminate substrate and SiC substrate. As stated above with respect to Claim 9, Eda et al. are silent with respect to these materials being used with a nitride III-V group

compound semiconductor. Rather, Eda et al. disclose only the use of GaAs or InP with such a semiconductor device.

Accordingly, Claim 10 is not obvious over Eda et al., and the rejection of Claim 10 under 35 U.S.C. §103 should be withdrawn.

Further, since Claims 10-12 depend from Claim 9, they are also patentably distinguishable over Eda et al. for the reasons cited above with respect to Claim 9.

With respect to new Claim 24, the Applicant submits that the applied prior art does not teach or suggest a semiconductor device, wherein the electrical connection to the semiconductor device is made directly through a via hole formed in the substrate.

Rather, Eda et al. disclose the semiconductor device 3 being disposed apart from the via hole and with electrical connections being made in some other indirect manner to the semiconductor device 3.

Therefore, Claim 24 is patentable.

If the Examiner believes that there is any issue which could be resolved by a telephone or personal interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee for such an extension is to be charged to Deposit Account No. 19-3140.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 3, the first full paragraph continuing to page 4, was amended as follows:

For thinning a GaAs substrate, [first conducted] primary lapping using a granular abrasive material of SiC or alumina is first conducted. Then, by using abrasive grains of a grain size of 1 μm or less of CeO_2, ZrO_2, CrO_2, or the like, the substrate is polished on a soft polisher such as synthetic resin or artificial leather to remove processing strain by lapping. As a result, the remainder depth of the processing strain is reduced to 10 μm or less, but additional processing by wet etching may be applied. As to the via hole to be made in the GaAs substrate, since GaAs is readily dissolved by any of sulfuric acid/hyrdogen peroxide solution or alkali solution, wet etching using such solution as the etchant is essentially sufficient for making the via hole. However, since side etching becomes large with wet etching and it is difficult to control the shape of the via hole, reactive ion etching (RIE) or ion milling is used normally. When using RIE for making the via hole, an etching rate as high as 50 to 100 μm/hr can be obtained, and the via hole can be made easily, by using a mixed gas of CCl_2F_2 and He as the etching gas and using a silicon oxide (SiO_2) film or an organic resist film as the etching mask. Since GaAs substrates are readily processed either mechanically or chemically as mentioned above, high-frequency operation and high-power output of GaAs FETs have already been realized by thinning the substrate and making the via hole in the substrate.

Page 4, the first full paragraph, continuing to page 5, was amended as follows:

However, it is difficult to employ the technique successfully used in GaAs FETs for thinning the substrate and making the via hole in the substrate also for fabrication of GaN FETs. As referred to above, sapphire substrates are often used for manufacturing GaN FETs. Sapphire, however, is much harder than

GaAs, and it [id] is extremely difficult to reduce the thickness of the sapphire substrate by using the above-explained conventional lapping technology. If it is forcibly thinned by lapping, it will form a large curve due to a lapping strain to be concave on the major surface side where the device should be made, and it will finally break down. Also regarding the via hole to be made in the sapphire substrate, since sapphire is very stable in chemical property, wet etching cannot be used without [any] an effective etchant. As to dry etching by RIE, since its etching rate is as very low as several μm/hr in maximum, and there is no etching mask [having a] being selectively acceptable for selective etching. Therefore, it is actually impossible to made the via hole with any of these methods. So, when making GaN FET on a sapphire substrate, it has been difficult to realize high-frequency operation and high-power output relying on thinning the substrate and making the via hole.

Page 7, the second full paragraph was amended as follows:

The [Inventor made researches,] present invention as summarized below, goes toward overcoming the above-indicated problems involved in the conventional techniques.

Page 7, the third full paragraph, continuing to page 8, was amended as follows:

For thinning a sapphire substrate already having formed a device using GaN semiconductors, there are some problems to solve. One of the problems is to thin the substrate sufficiently, namely to a thickness around 100 μm, for example, [decades] tens or μm, in the process of thinning the sapphire substrate by using lapping or some other method, without damaging the device on the surface of the substrate, while minimizing the processing strain and preventing warpage or breakage of the substrate. [when] When using a sapphire substrate, unlike the case using a GaAs substrate, warpage causes difficulties in subsequent processes unless substantially all of the strain in the thinned substrate is removed finally. Another problem is to find out an optimum processing method for making the via hole in any desired location of the sapphire substrate. Use of molten coral sand around 900 °C and use of molten phosphoric acid around 400 °C are known as methods for wet etching of sapphire. The [Inventor

made reviews to estimate] present invention estimates the applicability of these methods as a technique for making the via hole in a sapphire substrate and also to find out possible materials usable as an etching mask in the technique. The [Inventor further made researches to find out] present invention also discloses a new simple method for making the via hole without using the etching mask.

Page 10, the first full paragraph, continuing to page 11, and to page 12, was amended as follows:

For making the via hole, dry etching such as conventional RIE cannot be employed. Then, consideration is made on using the following method. That is, as shown in Fig. 2, for example, after growing a GaN semiconductor layer 2 with a thickness of several μm in total, for example, on the surface of a sapphire substrate 1, and a GaN FET 3 is formed on the GaN semiconductor layer 2. After that, a metal wiring and a pad for the GaN FET 3 are made. Reference numeral 4 denotes a Au pad electrically connected to the source of the GaN FET 3. Thereafter, an inter-layer insulating film 5 such as SiO_2 film is formed on the GaN semiconductor layer 2 to cover the Au pad 4. Subsequently, the sapphire substrate 1 is thinned to a thickness of 100 μm or less, for example to a thickness around [decades] tens of μm. After that, the bottom surface of the sapphire substrate 1 is covered locally at the location for the via hole by a multi-layered etching mask 6 made by stacking metal thin films. Used as the multi-layered film is, for example, a two-layered film stacking a thin film of a metal resistant to phosphoric acid, such as Pt, Au, Pd, or the like, on a thin film of a metal well [adhesive] adherent to the sapphire substrate, such as Ni, Cr, Ti, or the like. On the other hand, a protective film of polyimide 7, for example, is formed on the surface of the inter-layer insulating film 5. Thereafter, the bottom surface side of the sapphire substrate 1 is immersed into an etchant of phosphoric/sulfuric acid solution held at approximately 280 °C, for example, to etch it. In this case, since the etching rate is approximately 10 μm/hr, the etching time is adjusted depending upon the thickness of the sapphire substrate 1. In this manner, as shown in Fig. 3, the via hole 8 is made in the sapphire substrate 1. Then, next using RIE, part of the GaN semiconductor layer 2 exposed at the bottom of the via hole 8 is removed by etching to expose the Au pad 4 there. In the

process of etching the GaN semiconductor layer 2, if Cl_2 gas is sued as the etching gas, since the etching rate is 5 to 10 μm/hr and the ratio of the etching rate for Au is approximately 3 or more, a sufficient thickness of the Au pad 4 can be maintained even after etching the GaN semiconductor layer to a slightly over-etching level, if the Au pad 4 originally has a thickness around 1 μm or more. It may occur that the etching mask 6 on the bottom surface of the sapphire substrate 1 is removed while the GaN semiconductor layer 2 is etched by RIE. However, it is immaterial.

Page 19, the fourth full paragraph was amended as follows:

In the present invention, each nitride III-V compound semiconductor includes at least Ga and N, and may additionally include one or more group III elements selected from the group consisting of Al, In and B and/or one [ore] or more group V elements selected from the group consisting of As and P. Some specific examples of nitride III-V compound semiconductors are GaN, AlGaN, GaInN and AlGaInN.

Page 28, the first full paragraph was amended as follows:

Next as shown in Fig. 11, here again, by vacuum evaporation, for example, a 20 nm thick Cr film and a 5 μm thick Au film, for example, are sequentially stacked to form a Cr/Au film 36. Thereafter, a Au film 37 having a thickness as sufficiently thick as approximately 100 μm, for example, is made on the Cr/Au film 36 by plating, for example. [The] Then, the protective film 26 of polyimide is removed by an organic solvent.

IN THE CLAIMS:

The claims were amended as follows:

9. (Amended) A semiconductor device comprising:

[having] a single-crystal substrate made of a material different from nitride III-V compound semiconductors, and

a device [made] formed on one major surface of said single-crystal substrate by using III-V compound semiconductors, [comprising:]

wherein electrical connection to said device [being] is made through a via hole formed in said single-crystal substrate.

10. (Amended) The semiconductor device according to claim 9, wherein said single-crystal substrate is one of a sapphire substrate, spinel substrate, perovskite yttrium aluminate substrate [or] and SiC substrate.

12. (Amended) The semiconductor device according to claim 9 wherein said semiconductor device is [a] an FET using nitride III-V compound semiconductors.

Claim 24 was added.